Switching p-n diodes

Step response of resistive circuit
Step response of resistive circuit with the load having a parasitic parallel capacitance
Capacitance of the reverse biased p-n junction

The charge in the depletion region depends on the reverse bias:

$V_r = 0$

$\rho = 0$; $\rho = 0$;

$V_r < 0$

$\rho = 0$; $\rho = 0$;

Voltage-induced charge (positive)

Voltage-induced charge (negative)
Capacitance definitions

The **static** capacitance (per unit area),

\[ C_0 = \frac{Q_1}{V} \]

For the plain capacitor:

\[ V = \frac{Q_1}{\varepsilon \varepsilon_0} \times d \quad \Rightarrow \quad C_0 = \frac{\varepsilon \varepsilon_0}{d} \]

The **differential** capacitance (per unit area), which is the most important one:

\[ C_d = \frac{\partial Q_1}{\partial V} \]

For the plain capacitor,

\[ C_d = \frac{\varepsilon \varepsilon_0}{d} = C_0 \]
Differential capacitance of the p-n junction

\[ C_d = \frac{\partial Q_1}{\partial V} \]

Consider for simplicity an asymmetrical p-n junction:

\[ N_A \gg N_D; \quad \Delta Q = q \times N_D \times \Delta W \times A \]

\[ N_A \gg N_D, \quad V_{bi} - V_r = \frac{1}{2} \frac{q}{\varepsilon \varepsilon_0} N_D W^2 \]

Voltage increases \( \Rightarrow \) depletion region width \( W \) increases \( \Rightarrow \) the charge increases

\[ \frac{d |V_r|}{dW} = \frac{1}{2} \frac{q}{\varepsilon \varepsilon_0} N_D 2 \frac{W}{W} = \frac{q}{\varepsilon \varepsilon_0} N_D W \]

\[ \frac{dQ}{dW} = Aq N_D \]

\[ C_d = \frac{dQ}{d |V_r|} = \left( \frac{dQ}{dW} \right) \frac{d |V_r|}{dW} \]

\[ C_d = \frac{Aq N_D}{\varepsilon \varepsilon_0 N_D W} = \frac{\varepsilon \varepsilon_0 A}{W} \]

\[ C_d = \frac{\varepsilon \varepsilon_0 A}{W} \]

Same as plain capacitor with \( W \) plate separation
Reversed biased p-n junction as a variable capacitor

For the asymmetrical p$^+$ - n junction, 

$$N_A \gg N_D, \ V_{bi} - V_r = \frac{1}{2} \frac{q}{\varepsilon \varepsilon_0} N_D W^2$$

Voltage dependence of the space charge (depletion region) width
The capacitance associated with the diode,

\[ C = \frac{\varepsilon \varepsilon_0 A}{W} \]

(A is the diode area)

The series resistance of the diode of the total n-region thickness \( d \),

\[ R_S = \rho \frac{(d - W)}{A} \]

Since \( W \) is a function of \( V \), both \( C \) and \( R_S \) depend on \( V \)
Frequency tuning using a p-n junction capacitor (a varicap diode)

A simple bias circuit

35 mm x 35 mm x 60 mm

1 mm x 1 mm x 3 mm
**Pin-diode RF switches**

\[ C_t = \varepsilon A / W \]

\[ (V_{bi} - V_r) = \frac{1}{2} \frac{q}{\varepsilon \varepsilon_0} N_d W^2; \quad \text{Low } N_D \Rightarrow \text{Large } W \]
Pin-diode RF switches

Figure 2.13 High Power Broadband Antenna Switch

This switch can control 1 KW transmitter power with excellent distortion performance (IM3 < -80 dBC). The forward bias into Bias Terminal 1 is 1 Ampere, for low power dissipation in the transmitter diode and reverse bias of 500 Volts (at Bias Terminal 2) so that excessive RF current does not flow in the OFF state. HF Band (2 to 30 MHz) switches should use the UM2010 series and MF Band (0.3 to 3 MHz) switches should use the UM2310 series of PIN diodes.
Capacitance of Forward biased p-n junction

Forward biased junction stores an excessive charge $\Delta Q$:

$$\Delta Q_n = q \times A \times \int_0^\infty \Delta n_p (x) \, dx = q \times A \times n_{p0} \times \left( e^{qV/kT} - 1 \right) \times L_n$$

$$\Delta Q_p = q \times A \times \int_0^\infty \Delta p_n (x) \, dx = q \times A \times p_{n0} \times \left( e^{qV/kT} - 1 \right) \times L_p$$

The differential capacitance (also called *diffusion capacitance*):

$$C_d = \frac{\partial Q_{\text{stored}}}{\partial V}$$

$$\frac{\partial \Delta Q_n}{\partial V} = q \times A \times n_{p0} \times L_n \frac{q}{kT} e^{qV/kT}$$

$$\frac{\partial \Delta Q_p}{\partial V} = q \times A \times p_{n0} \times L_p \frac{q}{kT} e^{qV/kT}$$

![Diagram of p-n junction with charge storage](image)
Capacitance of Forward biased p-n junction (cont.)

The differential capacitance:

\[ C_d = \frac{\partial Q_{\text{stored}}}{\partial V} \]

\[ \frac{\partial \Delta Q_n}{\partial V} = q \times A \times n_{p0} \times L_n \frac{q}{kT} e^{qV/kT} \]
\[ \frac{\partial \Delta Q_p}{\partial V} = q \times A \times p_{n0} \times L_p \frac{q}{kT} e^{qV/kT} \]

\[ C_d = \frac{\partial \Delta Q_n}{\partial V} + \frac{\partial \Delta Q_p}{\partial V} = q \times A \times n_{p0} \times L_n \frac{q}{kT} e^{qV/kT} + q \times A \times p_{n0} \times L_p \frac{q}{kT} e^{qV/kT} \]

Compare this to the diode forward current:

\[ I = q \times A \times n_{p0} \times \left( e^{qV/kT} - 1 \right) \times L_n / \tau_n + q \times A \times p_{n0} \times \left( e^{qV/kT} - 1 \right) \times L_p / \tau_p \]

Assuming for simplicity \( \tau_n \approx \tau_p \) and \( V >> kT/q \):

\[ C_d = I \tau \frac{q}{kT} = I \tau / V_{Th} \]

Where \( V_{Th} = kT/q = 0.026 \text{ V at 300K} \)
P-n junction capacitance as a function of voltage

\[ C_d = \frac{\varepsilon \varepsilon_0 A}{W(V)} \]

\[ C_d = I \tau \frac{q}{kT} = I \tau / V_{Th} \]
TURN-ON OF A P-N DIODE

(a)

(b)

Current in the diode reaches $I_F$
Minority carrier density builds up on the n-side as the diode is forward biased.

Voltage across the diode builds up to its final value.
Turn-off of a p-n diode

![Diode schematic and current waveform](chart)

(a) Diode current in time

(b) Graph showing current and time intervals

- $i(t)$: Diode current
- $v(t)$: Voltage across the diode
- $R$: Resistance
- $V_F$: Forward voltage
- $V_R$: Reverse voltage
- $t_2$: Time interval
- $T/2$: Total time interval
- $\tau_{sd}$: Switching delay time
- $\tau_t$: Time constant
Turn-off of a p-n diode

Excess minority charge is removed in a time $\tau_{sd}$

Voltage across the diode remains positive until all of the excess minority charge is extracted. $\tau_{sd}$ is the storage delay time and $\tau_t$ is the RC time constant.
Equivalent circuit of a p-n diode (SPICE model)

Diode I-V

Diode capacitance =
Depletion region capacitance at $V < 0$;
Diffusion capacitance at $V > 0$