MOSFET I-V characteristics: general consideration

The current through the channel is

\[ I = \frac{V}{R} \]

where \( V \) is the DRAIN – SOURCE voltage.

Here, we are assuming that \( V \ll V_T \) (we will see why, later on).

The channel resistance, \( R \) (\( W \) is the device width):

\[ R = \frac{L}{q n \mu a W} = \frac{L}{q n_s \mu W} \]

where \( n_s = (c_i/q) \times (V_{GS} - V_T) \)

The channel current is:

\[ I = V \left( n_s \mu W \right) /L = V q \mu W (c_i/q) \times (V_{GS} - V_T) /L \]

\[ I = \mu W c_i \times (V_{GS} - V_T) V /L \]
MOSFET transconductance

In most MOSFET applications, an input signal is the gate voltage $V_G$ and the output is the drain current $I_d$. The ability of MOSFET to amplify the signal is given by the output/input ratio: the transconductance, $g_m = dI/dV_{GS}$.

$$I = \mu W c_i \times (V_{GS} - V_T) \frac{V}{L} \quad \text{(V is the Drain – Source voltage)}$$

From this: $g_m = V \mu W c_i / L$

Key factors affecting FET performance (for any FET type):

- High carrier mobility $\mu$ and short gate length $L$ are the key features of FETs
Modern submicron gate FET

Operating frequency – up to 300 GHz
When no drain voltage $V$ is applied, the entire channel has the same potential as the Source, i.e. $V_{CH} = 0$.

In this case, as we have seen, $n_S = \left( \frac{c_i}{q} \right) \times (V_{GS} - V_T)$

where $V_{GS}$ is the gate – source voltage and $V_T$ is the threshold voltage.

When the drain voltage $V$ is applied, the channel potential changes from $V_{CH} = 0$ on the Source side to $V_{CH} = V$ on the drain side.

In this case, the induced concentration in the channel also depends on the position.
With the drain voltage $V$ is applied, the actual induced concentration in any point $x$ of the channel depends on the potential difference between the gate and the channel potential $V(x)$ at this point. This is because this local potential difference defines the voltage that charges the elementary gate – channel capacitor.

On the source end of the channel ($x=0$, $V_{CH}=0$):

$$n_S(0) = \frac{c_i}{q} \times (V_{GS} - V_T).$$

On the drain end of the channel ($x=L$, $V_{CH}=V$):

$$n_S(L) = \frac{c_i}{q} \times (V_{GS} - V_T - V) \leq n_S(0)$$

At any point between source and drain,

$$n_S(L) < n_S(x) = \frac{c_i}{q} \times [V_{GS} - V_T - V(x)] < n_S(0)$$
Drain current saturation in MOSFET

Semiconductor

\[ V_{GS} > V_T \]

\[ V = 0 \]

\[ V_1 > 0 \]

\[ V_2 > V_1 \]

\[ V_3 = V_{GS} - V_T \]
MOSFET Modeling

1. Constant mobility model

Assuming a constant electron mobility, $\mu_n$, using the simple charge control model the absolute value of the electron velocity is given by,

$$v_n = \mu_n F = \mu_n \frac{dV}{dx}$$

With the gate voltage above the threshold, the drain current, $I_d$, is given by

$$I_d = W q \mu_n \frac{dV}{dx} n_s$$

Where $W$ is the device width

Rewriting,

$$\frac{dV}{dx} = \frac{I_d}{W \mu_n c_i (V_{GT} - V)}$$

Where $V_{GT} = V_{GS} - V_T$.

$dV$ vs $dx$ dependence represents a series connection of the elementary parts of MOSFET channel (for the series connection, voltages add up whereas current is the same).
Integrating along the channel, from $x=0$ ($V=0$) to $x=L$ ($V=V_{DS}$), we obtain:

$$I_d = \frac{W \mu_n c_i}{L} V_{GT} V_{DS}$$  \quad \text{Linear region}

For, $V_{DS} \ll V_{GT}$,

$$I_d = \frac{W \mu_n c_i}{L} V_{GT} V_{DS}$$  \quad \text{Linear region}

For, larger $V_{DS}$,

$$I_d = \frac{W \mu_n c_i}{L} \left( V_{GT} - \frac{V_{DS}}{2} \right) V_{DS}$$  \quad \text{Sub-linear region}
Channel pinch off and current saturation

Pinch off occurs when $V_G - V_{CH} = V_T$ at the drain end; $n_S (L) = 0$; the current $I_d$ saturates

When,

$$V_{DS} = V_{SAT} = V_{GS} - V_T$$

where $V_{SAT}$ is the saturation voltage.

From the $I_d - V$ dependence,

at $V_{DS} = V_{SAT} = V_{GT}$,

$$I_d = \frac{W \mu n c_i}{L} \left( V_{GT} - \frac{V_{DS}}{2} \right) V_{DS}$$

The saturation (pinch off) current,

$$I_d = I_{Sat} = \frac{W \mu n c_i}{2L} V_{GT}^2$$
Transconductance

Defined as

\[ g_m = \left. \frac{dI_d}{dV_{GS}} \right|_{V_{DS}} \]

From the equations for the drain current, \( I_d \), derived above, we find that

\[ g_m = \begin{cases} \beta V_{DS}, & \text{for } V_{DS} \ll V_{SAT} \\ \beta V_{GT}, & \text{for } V_{DS} > V_{SAT} \end{cases} \]

where \( \beta = \mu_n c_i \frac{W}{L} \)

High transconductance is obtained with high values of
the low field electron mobility, thin gate insulator layers
(i.e., larger gate insulator capacitance \( c_i = \varepsilon_i/d_i \)), and
large \( W/L \) ratios.
2. Velocity saturation model

In semiconductors, electric field $F$ accelerates electrons, i.e. the drift velocity of electron increases: $v = \mu F$

However, at high electric fields this velocity saturates.

In modern short channel devices with channel length of the order of 1 µm or less, the electric field in the channel can easily exceed the characteristic electric, $F_s$, field of the velocity saturation:

$$F_s = \frac{\nu_s}{\mu n}$$
Electric field in the channel

the electric field in the channel in the direction parallel to the semiconductor-insulator interface

\[ F = \frac{I_d}{q\mu_n n_s (V) W} \quad \text{and} \quad \nu_n = \mu_n F = \mu_n \frac{dV}{dx} \]

Potential, electric field, and surface electron concentration in the channel of a Si MOSFET for \( V_{DS} = 1 \) and 1.2 V. \( L = 5 \mu\text{m}, \, d_i = 200 \text{Å}, \, \mu n = 800 \text{cm}^2/\text{Vs}, \, V_{GS} = 2 \text{V}, \, V_T = 1 \text{V}. \)
Once the electric field at the drain side of the channel (where the electric field is the highest) exceeds $F_s$, the electron velocity saturates, leading to the current saturation.

In short-channel MOSFETs, this occurs at the drain bias smaller than the pinch-off voltage $V_{DS} = V_{GT}$.

$$\int dV = \frac{I_d}{W \mu_n c_i (V_{GT} - V)} dx$$

Field at drain

$$F(L) = \left. \frac{dV}{dx} \right|_{x=L} = \frac{I_d}{W \mu_n c_i (V_{GT} - V_{DS})}$$

Saturation condition,

$$F_s = \frac{I_{SAT}}{\mu n c_i (V_{GT} - V_{SAT}) W}$$
Saturation current versus gate-to-source voltage for 0.5 µm gate and 5 µm gate MOSFETs. Dashed lines: constant mobility model, solid lines: velocity saturation model.
MOSFET saturation current accounting for velocity saturation:

\[ I_{sat} = \frac{g_{ch}V_{GT}}{1 + \sqrt{1 + \left(\frac{V_{GT}}{V_L}\right)^2}} \]

where \( V_L = F_sL \) and the channel conductance \( g_{ch} = q \mu_n n_s W / L \),

where \( n_s = c_i V_{GT}/q \)

When \( F_sL >> V_{GT} \) (MOSFET with long gate or no velocity saturation):

\[ I_{sat} \approx \frac{g_{ch}}{2} V_{GT} \]

\[ I_d = I_{sat} = \frac{W \mu_n c_i}{2L} V_{GT}^2 \]

(Expression obtained before on slide 9)

When \( F_sL << V_{GT} \) (MOSFET with short gate or early velocity saturation):

\[ I_{sat} \approx g_{ch} V_L \]

(Note that \( g_{ch} \) is controlled by \( V_{GT} \))
Source and drain series resistances.

Source and drain parasitic series resistances, $R_s$ and $R_d$, play an important role, especially in short channel devices where the channel resistance is smaller.

\[ V_{ds} = I_d R_s + V_{DS} + I_d R_d \]

\[ V_{GS} = V_{gs} - I_d R_s \]

\[ V_{DS} = V_{ds} - I_d (R_s + R_d) \]
The measured transconductance (extrinsic)

\[ g_m = \left. \frac{dI_d}{dV_{gs}} \right|_{V_{ds}=\text{const}} \]

The intrinsic transconductance (\(V_{GS}\) and \(V_{DS}\) being intrinsic voltages)

\[ g_{mo} = \left. \frac{dI_d}{dV_{GS}} \right|_{V_{DS}=\text{const}} \]

These parameters are related as

\[ g_m = \frac{g_{mo}}{1 + g_{mo} R_s + g_{do} (R_s + R_d)} \]

Where \(g_{d0}\) is the drain conductance

\[ g_{do} = \left. \frac{dI_d}{dV_{DS}} \right|_{V_{GS}=\text{const}} \]

In the current saturation region (\(V_{DS} > V_{SAT}\), \(g_{d0} \approx 0\)

Similarly, extrinsic drain conductance can be written as,

\[ g_d = \frac{g_{do}}{1 + g_{mo} R_s + g_{do} (R_s + R_d)} \]
The saturation current in MOSFET with parasitic resistances:

\[ I_{sat} = \frac{g_{cho} V_{gt}}{1 + g_{cho} R_s + \sqrt{1 + 2g_{cho} R_s + \left(\frac{V_{gt}}{V_L}\right)^2}} \]

where \( V_L = F_s L \) and \( g_{cho} = c_i V_{gt} \mu_n W/L \).

MOSFET output characteristics calculated for zero parasitic resistances and parasitic resistances of 5 \( \Omega \). Gate length is 1 \( \mu \text{m} \).
MOSFET capacitance-voltage characteristics

To simulate MOSFETs in electronic circuits, we need to have models for both the current-voltage and the capacitance-voltage characteristics.

As MOSFETs is a three terminal device, we need three capacitances: $C_{gs}$, $C_{gd}$ and $C_{ds}$.

Capacitance (differential) is defined as $C = \frac{dQ}{dV}$. For example,

$$C_{gs} = \frac{dQ_s}{dV_{gs}}$$
(where $Q_s$ is the channel charge between S and G)

Therefore, the total channel charge $Q_N$ has to be divided (partitioned) between the source and drain charges. How should we partition $Q_N$ between $Q_s$ and $Q_d$?

It is clear from the device symmetry that at zero drain bias $Q_s = Q_d$. If the total channel charge is $Q_N$, then $Q_s = 0.5 \ Q_N$ and $Q_d = 0.5 \ Q_N$. 
In the saturation regime, the charge distribution is no longer symmetrical: \( Q_s > Q_d \)

In this case, we let \( Q_s = F_p Q_N \) and \( Q_d = (1 - F_p) Q_N \), where \( F_p \) is the partitioning factor. In saturation, \( F_p > 0.5 \)

The challenge using this model is to determine \( F_p \) as a function of \( V_{gs} \) and \( V \)
Meyer model for MOSFET capacitance (used in SPICE)

\[
C_{gs} = \frac{2}{3} C_i \left[ 1 - \left( \frac{V_{GT} - V_{DS}}{2V_T - V_{DS}} \right)^2 \right] + C_f
\]

\[
C_{gd} = \frac{2}{3} C_i \left[ 1 - \left( \frac{V_{GT}}{2V_T - V_{DS}} \right)^2 \right] + C_f
\]

\( C_i = c_i \times W \times L \) is the channel capacitance

The capacitance \( C_f \) is the fringing capacitance.

\[ C_f \approx \beta_c \varepsilon_s W \]

where \( \beta_c \approx 0.5 \)

In saturation, \( V_{DS} \) has to be replaced by \( V_{SAT} \) (where \( V_{SAT} = V_{GT} \))

This results in

\[ C_{GS\,SAT} = \frac{2}{3} C_i + C_f; \]

\[ C_{Gd\,SAT} = C_f \]
Meyer model for MOSFET capacitance (used in SPICE)