The J-K flip-flop is the most versatile of the basic flip-flops. It has the input-following character of the clocked D flip-flop but has two inputs, traditionally labeled J and K. If J and K are different then the output Q takes the value of J at the next clock edge.

If J and K are both low then no change occurs. If J and K are both high at the clock edge then the output will toggle from one state to the other. It can perform the functions of the set/reset flip-flop and has the advantage that there are no ambiguous states. It can also act as a T flip-flop to accomplish toggling action if J and K are tied together. This toggle application finds extensive use in binary counters.

A simplified version of the versatile J-K flip-flop. Note that the outputs feed back to the enabling NAND gates. This is what gives the toggling action when J=K=1.
Switching Example: J-K Flip-Flop

The positive going transition (PGT) of the clock enables the switching of the output Q. The "enable" condition does not persist through the entire positive phase of the clock. The J & K inputs alone cannot cause a transition, but their values at the time of the PGT determine the output according to the truth table. This is an application of the versatile J-K flip-flop.

Truth Table

<table>
<thead>
<tr>
<th>J</th>
<th>K</th>
<th>CLK</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>↑</td>
<td>Q</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>↑</td>
<td>Q</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>↑</td>
<td>Q</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>↑</td>
<td>Q</td>
</tr>
</tbody>
</table>

Output toggles at each PGT if J & K both high.
Output makes transition to Q value if J ⊕ K
Would switch to high, but it is already high, so no transition
Output toggle since J=K=1
No change when J=K=0

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Go Back
In synchronous data transfer between two J-K flip-flops, a transfer signal on the clock input causes transfer from cell A to cell B. The transfer signal could be applied to several such cells in series to create a shift register.

In asynchronous data transfer, a transfer pulse may be applied at any time to force the data onto the asynchronous set and clear inputs, storing the data regardless of what is happening on the other inputs.